

1 Off-line LED Driver using CPC9909

This application note provides general guidelines for designing an off-line LED driver using Clare's CPC9909.

The CPC9909 features pulse frequency modulation (PFM) with a constant peak-current control scheme. This regulation scheme is inherently stable, allowing the driver to be operated above 50% duty cycle without open-loop instability or sub-harmonic oscillations.

The CPC9909 has two current sense thresholds: one is internally set at 250mV, and the other can be externally set at the LD pin. The lower of these two thresholds, in

conjunction with the current sense resistor (R_{sense}) at the CS pin, determines the LED peak current.

A linear dimming function can be accomplished by adjusting the current sense threshold voltage in the range of 0-270mV. When the linear dimming function is not used, it is recommended that the LD pin be connected to V_{DD} .

Figure 1 shows the functional block diagram of the CPC9909 device. **Figure 2** shows a schematic of a typical application circuit for the device, which is referred to in all the discussions that follow.

Figure 1 CPC9909 Block Diagram

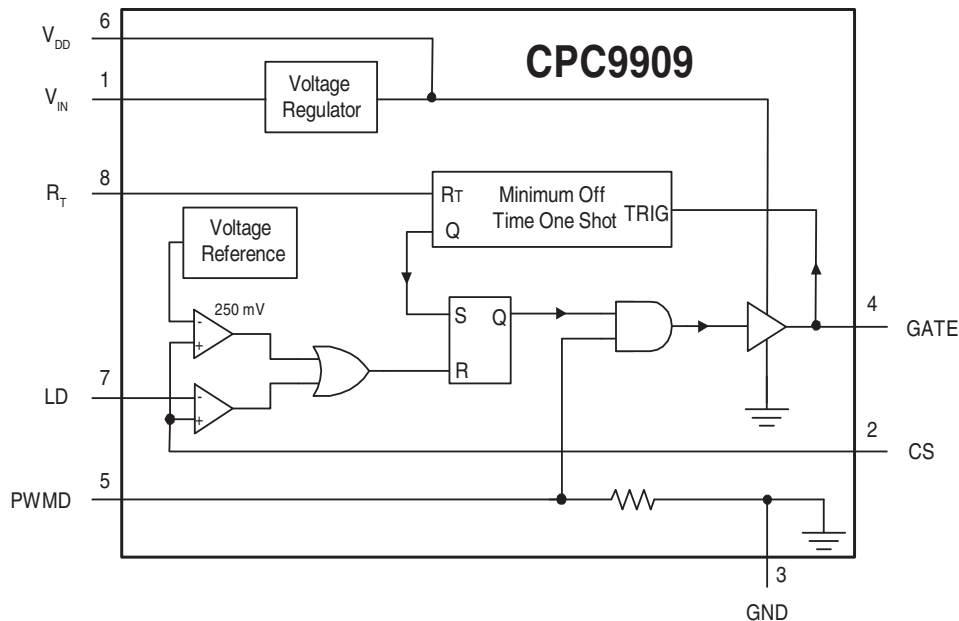
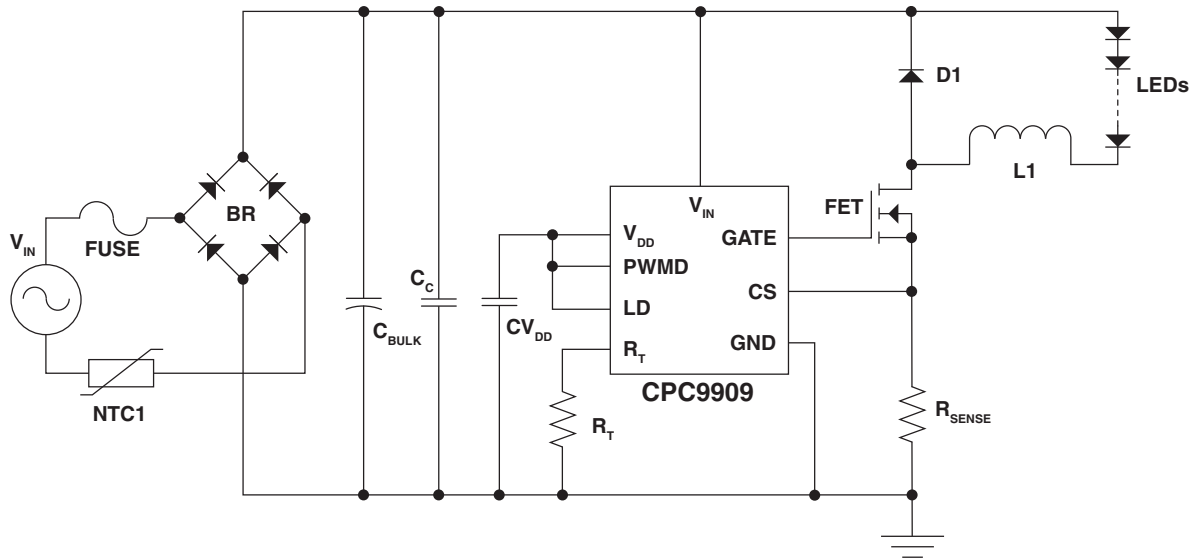


Figure 2 Application Circuit Diagram



2 Typical Design Parameters

Parameter	Symbol	Min	Typ	Max	Units
AC Input Voltage					
Minimum Voltage	V_{AC-min}	90	-	-	V_{rms}
Maximum Voltage	V_{AC-max}	-	-	130	
AC Input Frequency	f_{AC}	50	-	60	Hz
LED String Voltage	$V_{LEDstring}$	-	90	-	V
LED String Current	I_{LEDmax}	-	-	350	mA
Estimated Efficiency	η	-	0.90	-	-
Oscillator Frequency	f_S	-	53	-	kHz

- Output Power Calculation

$$P_{OUT} = V_{LEDstring} \cdot I_{LEDmax}$$

$$P_{OUT} = 90V \cdot 350mA$$

$$P_{OUT} = 31.5W$$

- Input Power Calculation

$$P_{IN} = \frac{P_{OUT}}{\eta}$$

$$P_{IN} = \frac{31.5W}{0.90}$$

$$P_{IN} = 35W$$

- DC Bulk Voltage at Low and High Line

$$V_{DC_bulk_min} = \sqrt{2} \cdot V_{AC-min}$$

$$V_{DC_bulk_min} = 127.3V$$

$$V_{DC_bulk_max} = \sqrt{2} \cdot V_{AC-max}$$

$$V_{DC_bulk_max} = 183.8V$$

- Average Input Current

$$I_{in_avg} = \frac{P_{in}}{V_{DC_bulk_min}} = \frac{35W}{127.3V}$$

$$I_{in_avg} = 0.275A$$

- Peak Input Current

$$I_{in_pk} = 5 \cdot I_{in_avg}$$

$$I_{in_pk} = 1.375A$$

Note: During a surge, the current could be as much as 5 times higher, hence the multiplier.

3 Duty Cycle

From the design requirements, the duty cycle can be calculated as:

$$D = \frac{V_{LEDstring}}{V_{DC_bulk_min}} = \frac{90V}{127.3V}$$

$$D = 0.707$$

4 Switching Frequency and Resistor R_T Selection

It is recommended that the switching frequency for off-line applications be between 30kHz and 120kHz.

The CPC9909 requires an external resistor, R_T , that sets the one-shot minimum off-time. The off-time can be determined by:

$$t_{off} = \frac{R_T}{66} + 0.8$$

Where t_{off} is the off-time in microseconds, and R_T is in $k\Omega$. As an example, if R_T is set to $309k\Omega$, t_{off} is then:

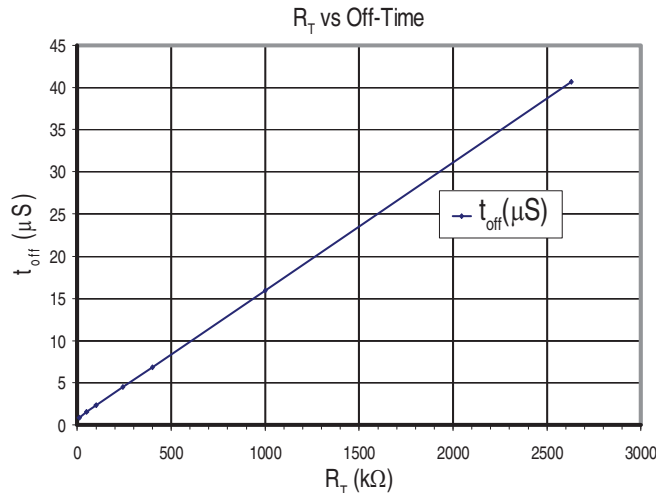
$$t_{off} = \frac{309k\Omega}{66} + 0.8 = 5.482\mu s$$

Off-time selection indirectly determines the switching frequency, f_S , of the LED driver. The switching frequency in the above example is determined by:

$$f_S = \frac{1-D}{t_{off}} = \frac{1-0.707}{5.482\mu s} = 53kHz$$

where D =Duty Cycle.

Figure 3 Resistor Value vs. Off-Time



5 Selecting Fuse and NTC1 Thermistor

The fuse protects the circuit from input current surges during turn-on. Choose a fuse that is rated five times the peak input current.

$$I_{fuse} = 5 \cdot I_{in_pk}$$

$$I_{fuse} = 6.875A$$

The thermistor in series with the input bridge rectifier limits the inrush charging current into the input bulk capacitor during startup. The value is determined by:

$$R_{th_cold} = \frac{\sqrt{2} \cdot V_{AC_max}}{I_{in_pk}}$$

$$R_{th_cold} = 133.7\Omega$$

6 Diode Bridge Rectifier

The selection of the diode bridge rectifier is based on DC blocking voltage, forward current, and surge current.

$$V_{rb} = V_{DC_bulk_max}$$

$$V_{rb} = 183.8V$$

The diode forward current rating should be set to 1.5 times the input average current.

$$I_{fb} = 1.5 \cdot I_{in_avg}$$

$$I_{fb} = 0.4125A$$

The diode bridge can be subjected to currents as high as 5 times the forward current, and the diode bridge should be rated accordingly.

$$I_{fsb} = 5 \cdot I_{fb}$$

$$I_{fsb} = 2.0625A$$

7 Input Bulk Capacitor, C_{bulk} , and C_C

The AC line voltage is filtered by the input bulk capacitor (C_{bulk}), which is selected based on the minimum peak rectifier input line voltage and peak-to-peak ripple voltage. Assuming a 20% ripple:

$$r_{DC_bulk} = 0.2$$

$$V_{in_min} = (1 - r_{DC_bulk}) \cdot V_{DC_bulk_min} = (1 - 0.2) \times (127.3)$$

$$V_{in_min} = 101.8V$$

$$C_{bulk} = \frac{P_{in}}{f_{AC} \cdot (V_{DC_bulk_min}^2 - V_{in_min}^2)}$$

$$C_{bulk} = \frac{35W}{60Hz \cdot (127.3V^2 - 101.8V^2)}$$

$$C_{bulk} = 100\mu F$$

For this example, the voltage rating of the capacitor should be more than $V_{DC_bulk_max}$ with some safety margin factored in. An electrolytic capacitor with a 250V, 100 μ F rating would be adequate.

Note that electrolytic bulk capacitors contain parasitic elements that cause their performance to be less than ideal. One important parasitic is the capacitor's Equivalent Series Resistance (ESR), which causes internal heating as the ripple current flows into and out of the capacitor. In order to select a proper capacitor, the designer should consider capacitors that are specifically designed to endure the ripple current at the maximum temperature, and that have an ESR that is guaranteed within a specific frequency range (usually provided by manufacturers in the 120Hz to 100kHz range).

The Effective Series Inductance (ESL) is another parasitic that limits the effectiveness of the electrolytic capacitor at high frequencies.

The combination of the variation of ESR over temperature and a high ESL may require adding a parallel film or tantalum capacitor (C_C) to absorb the high-frequency ripple component. This keeps the combined ESR within the required limit over the full design temperature range.

8 Bypass Capacitor, CV_{DD}

The V_{DD} pin is the internal regulator's output pin and must be bypassed by a low-ESR capacitor (typically 0.1 μ F or higher) to provide a low-impedance path for high-frequency switching noise.

9 Inductor Design

The inductor (L1) value is determined based on desired LED ripple current and the switching frequency. 53 kHz was chosen as the optimum switching frequency to minimize switching losses, and to reduce circuit power dissipation at the expense of larger inductor size.

Assuming a 30% peak-to-peak ripple in LED current, one can calculate the inductor requirements:

$$r_{iout} = 0.3$$

$$L_{min_buck} = \frac{V_{LEDstring} \cdot t_{off}}{r_{iout} \cdot I_{LEDmax}}$$

$$L_{min_buck} = \frac{90V \cdot 5.482\mu s}{0.3 \cdot 350mA}$$

$$L_{min_buck} = 4.7mH$$

Inductor peak current rating:

$$I_{Lmax} = I_{LEDmax} \cdot (1 + (0.5 \cdot r_{iout}))$$

$$I_{Lmax} = 350mA \cdot (1 + (0.5 \cdot 0.3))$$

$$I_{Lmax} = 0.403A$$

In some cases, when the design requires a higher current rating and there is no standard inductor available, a custom-made inductor should be considered.

10 Power MOSFET and Diode Selection

The peak voltage seen by the discrete power MOSFET (FET) and diode (D1) are equal to the maximum bulk voltage. For safety reasons assume an additional 50% margin by design.

$$V_{FET_BVDSS_buck} = 1.5 \cdot V_{DC_bulk_max}$$

$$V_{FET_BVDSS_buck} = 1.5 \cdot 183.8V$$

$$V_{FET_BVDSS_buck} = 275.771V$$

$$V_{Diode_r_buck} = 1.5 \cdot V_{DC_bulk_max}$$

$$V_{Diode_r_buck} = 1.5 \cdot 183.8V$$

$$V_{Diode_r_buck} = 275.771V$$

The maximum RMS current through the FET depends on the maximum duty cycle seen by the FET. In this buck converter, the maximum duty cycle is set to 70.7%. Choose a MOSFET with a rating of 3 times this current.

$$I_{FET_rms_buck} = 0.707 \cdot I_{LEDmax}$$

$$I_{FET_rating_buck} = 3 \cdot I_{FET_rms_buck}$$

$$I_{FET_rating_buck} = 0.883A$$

The average current through the diode is one-half of the LED current. Choose a diode with a rating 3 times this current.

$$I_{Diode_buck} = 0.707 \cdot I_{LEDmax} = 0.707 \cdot 350mA = 0.247A$$

$$I_{Diode_rating_buck} = 3 \cdot I_{Diode_buck}$$

$$I_{Diode_rating_buck} = 0.742A$$

For this design, the IXTA8N50P external power FET, in the SMD D2-Pak package, was selected from the IXYS' family of Polar N-channel devices. The Polar process features 30% reduction of $R_{DS(on)}$, and a substantial reduction of total gate charge, Q_G . This helps with improved LED driver efficiency by minimizing conduction and switching losses. In addition, the Polar power FET family has very low thermal resistance, $R_{\theta JC}$, which improves the device's power dissipation. The IXA8N50P can be used with an external heat sink similar to Aavid Thermalloy's part number 573100.

The high frequency switching of the buck LED driver requires the use of a fast recovery diode. The BYV26_B series diode, in the SOD-57 package, was chosen for this design.

11 Current Sense Resistor, R_{sense}

The current sense resistor (R_{sense}) is selected based on the desired LED current. In this case, the maximum LED current is set at 350mA. Note that there is a difference between the peak current and the average current in the inductor. This ripple difference should be included in resistor calculations. The current sense threshold is given in the CPC9909 data sheet.

Assuming 30% ripple:

$$V_{cs(high)} = 250mV$$

$$r_{iout} = 0.3$$

$$R_{sense} = \frac{V_{cs(high)}}{(1 + (0.5 \cdot r_{iout})) \cdot I_{LEDmax}} = \frac{250mV}{(1 + (0.5 \cdot 0.3)) \cdot 350mA}$$

$$R_{sense} = 0.621\Omega$$

Note that since the current sense threshold voltage of the CPC9910 ($V_{cs(high)}$) is specified between 200mV and 300mV, 250mV, the nominal value, is used in the formula above.

Power dissipation across the sense resistor:

$$P = I_{LEDmax}^2 \cdot R_{sense}$$

$$P = 0.076W$$

In practice, select a resistor power rating that is at least twice the calculated value.

12 Layout Considerations

In all switching converters, proper grounding and trace length are important considerations. The LED driver operates at a high frequency, and the designer must keep trace length from the CPC9909 GATE pin to the external power MOSFET as short as possible. Doing this helps to avoid such undesirable performance characteristics as ringing and spiking.

In high-frequency switching, current tends to flow near the surface of a conductor, so ground traces on the PC board must be wide in order to avoid any problems due to parasitic trace inductance. If possible, one side of the PC board should be used as a ground plane.

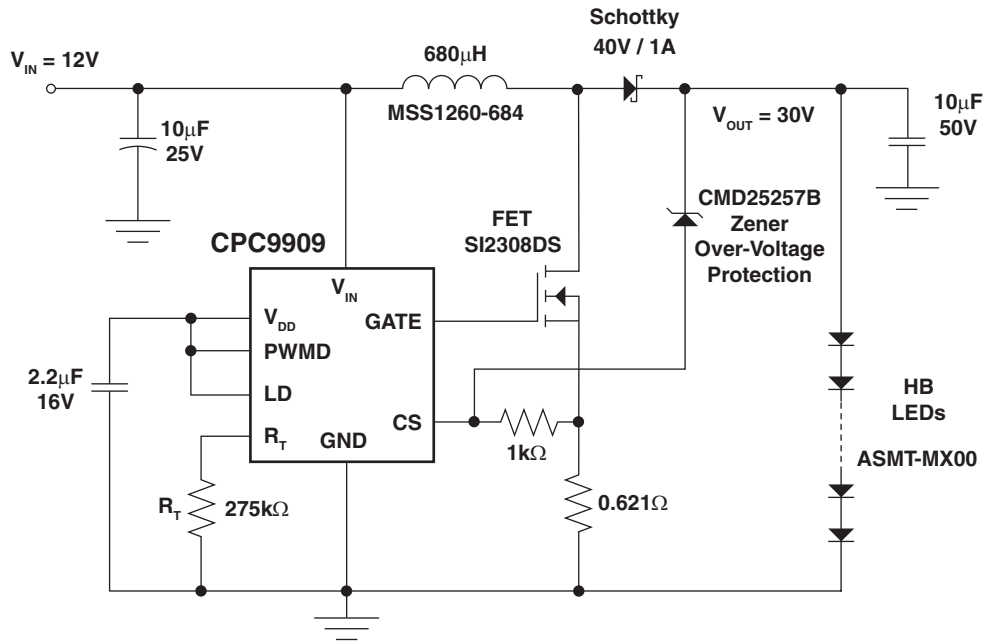
The current sense resistor, R_{sense} , should be kept close to the CS pin in order to prevent noise coupling to the internal high-speed voltage comparator, which would affect IC performance. In addition, R_T should be placed away from the inductor and away from any PCB trace that is close to switching noise.

13 Application Suggestion

The CPC9909 provides stable operation at above 50% duty cycle, which makes this driver well suited to

operation in boost configuration. The circuit below has optional open-LED protection.

Figure 4 Boost Configuration Circuit



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